REMARKS

Claim Rejections

Claims 1-11, 13 and 14 are rejected under 35 U.S.C. § 102(e) as being anticipated by Broberg, III et al. (U.S. 6,601,122, hereinafter Broberg). Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Broberg in view of Godfrey (U.S. 6,889,279).

Drawings

It is noted that the Examiner has accepted the drawings as originally filed with this application.

Claim Amendments

By this Amendment, Applicant has amended claim 1 of this application. It is believed that the amended claims specifically set forth each element of Applicant's invention in full compliance with 35 U.S.C. § 112, and define subject matter that is patentably distinguishable over the cited prior art, taken individually or in combination.

The primary reference to Broberg teaches exceptions and interrupts with a dynamic priority and vector routing. Broberg teaches an override address register in the processing unit. In Broberg, when an interruption occurs, the CPU will fetch the interrupt service routine from the override address instead of the default address (claim 1). In other words, the override address of Broberg is different from the default address of the present invention (claim 6b). Moreover, since Broberg places the interrupt service routine into the on-chip high-speed memory of the processing unit, an interrupt latency and an interrupt service time will be reduced. It should be noticed that the present invention only places the interrupt vector table into the high speed-memory, so as to reduce the interrupt latency.

In summary, the present invention places the interrupt vector table into the high-speed memory, whereas Broberg places the interrupt service routine into the on-chip high-speed memory.

In the present invention, the low-speed and high-speed memories both store an interrupt vector table individually for recording at least one entry instruction of an interrupt service routine. When an interruption occurs, the CPU generates an interrupt vector address for the memory controller, and if the re-addressing device of the memory controller identifies that the address falls within an address range of the interrupt vector table, the re-addressing device sends out an enable signal to the high-speed memory to enable the CPU to fetch the corresponding entry instruction of the interrupt service routines in the high-speed memory, instead of the predetermined low-speed memory (claim 1 of the present invention). The present invention is deigned to make the CPU fetch the interrupt vector table from the high-speed memory instead of the low-speed memory, and the high-speed memory only stores the interrupt vector table without the interrupt service routine. The present invention does not have a mechanism of an override address and is different from the default address of Broberg.

Broberg does not teach the low-speed and high-speed memories both storing an interrupt vector table individually for recording at least one entry instruction of an interrupt service routine; nor does Broberg teach, when the interruption occurs, the CPU generates an interrupt vector address for the memory controller, and when the re-addressing device of the memory controller identifies that the interrupt vector address falls within the address range of the interrupt vector table, the re-addressing device sending an enable signal to the high-speed memory enabling the CPU to fetch the corresponding entry instruction of the interrupt service routines stored in the high-speed memory.

It is axiomatic in U.S. patent law that, in order for a reference to anticipate a claimed structure, it must clearly disclose each and every feature of the claimed structure. Applicant submits that it is abundantly clear, as discussed above, that Broberg does not disclose each and every feature of Applicant's amended claims and, therefore, could not possibly anticipate these claims under 35 U.S.C. § 102. Absent a specific showing of these features, Broberg cannot be said to anticipate any of Applicant's amended claims under 35 U.S.C. § 102.

The secondary reference to Godfrey teaches a pre-stored vector interrupt handling system and is cited for teaching an ARM processor.

Godfrey does not teach the low-speed and high-speed memories both storing an interrupt vector table individually for recording at least one entry instruction of an interrupt service routine; nor does Godfrey teach, when the interruption occurs, the CPU generates an interrupt vector address for the memory controller, and when the re-addressing device of the memory controller identifies that the interrupt vector address falls within the address range of the interrupt vector table, the re-addressing device sending an enable signal to the high-speed memory enabling the CPU to fetch the corresponding entry instruction of the interrupt service routines stored in the high-speed memory.

Even if the teachings of Broberg and Godfrey were combined, as suggested by the Examiner, the resultant combination does not suggest: the low-speed and high-speed memories both storing an interrupt vector table individually for recording at least one entry instruction of an interrupt service routine; nor does the combination suggest, when the interruption occurs, the CPU generates an interrupt vector address for the memory controller, and when the re-addressing device of the memory controller identifies that the interrupt vector address falls within the address range of the interrupt vector table, the re-addressing device sending an enable signal to the high-speed memory enabling the CPU to fetch the corresponding entry instruction of the interrupt service routines stored in the high-speed memory.

It is a basic principle of U.S. patent law that it is improper to arbitrarily pick and choose prior art patents and combine selected portions of the selected patents on the basis of Applicant's disclosure to create a hypothetical combination which allegedly renders a claim obvious, unless there is some direction in the selected prior art patents to combine the selected teachings in a manner so as to negate the patentability of the claimed subject matter. This principle was enunciated over 40 years ago by the Court of Customs and Patent Appeals in In re Rothermel and Waddell, 125 USPQ 328 (CCPA 1960) wherein the court stated, at page 331:

> The examiner and the board in rejecting the appealed claims did so by what appears to us to be a piecemeal reconstruction of the prior art patents in the light of appellants' disclosure. ... It is easy now to attribute to this prior art the knowledge which was first made available by appellants and then to assume that

> it would have been obvious to one having the ordinary skill in the art to make these suggested reconstructions. While such a reconstruction of the art may be an alluring way to rationalize a rejection of the claims, it is not the type of rejection which the statute authorizes.

The same conclusion was later reached by the Court of Appeals for the Federal Circuit in Orthopedic Equipment Company Inc. v. United States, 217 USPQ 193 (Fed.Cir. 1983). In that decision, the court stated, at page 199:

> As has been previously explained, the available art shows each of the elements of the claims in suit. Armed with this information, would it then be non-obvious to this person of ordinary skill in the art to coordinate these elements in the same manner as the claims in suit? The difficulty which attaches to all honest attempts to answer this question can be attributed to the strong temptation to rely on hindsight while undertaking this evaluation. It is wrong to use the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit. Monday morning quarterbacking is quite improper when resolving the question of non-obviousness in a court of law.

In In re Geiger, 2 USPQ2d, 1276 (Fed.Cir. 1987) the court stated, at page 1278:

> We agree with appellant that the PTO has failed to establish a *prima facie* case of obviousness. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching suggestion or incentive supporting the combination.

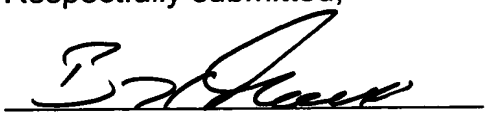
Applicant submits that there is not the slightest suggestion in either Broberg or Godfrey that their respective teachings may be combined as suggested by the Examiner. Case law is clear that, absent any such teaching or suggestion in the prior art, such a combination cannot be made under 35 U.S.C. § 103.

Neither Broberg nor Godfrey disclose, or suggest a modification of their specifically disclosed structures that would lead one having ordinary skill in the art to arrive at Applicant's claimed structure. Applicant hereby respectfully submits that no combination of the cited prior art renders obvious Applicant's amended claims.

Summary

In view of the foregoing amendments and remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

Date: October 3, 2005 By: 

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